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APPLICATION FOR LETTERS PATENT

for

**SURFACE BARRIERS FOR COPPER AND SILVER INTERCONNECTS PRODUCED BY  
A DAMASCENE PROCESS**

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## TITLE OF THE INVENTION

### SURFACE BARRIERS FOR COPPER AND SILVER INTERCONNECTS PRODUCED BY A DAMASCENE PROCESS

## CROSS-REFERENCE TO RELATED APPLICATION

**[0001]** This application is a divisional of application Serial No. 10/414,147, filed April 15, 2003, pending.

## BACKGROUND OF THE INVENTION

**[0002]** Field of the Invention: The present invention relates to a method of fabricating a barrier layer and, more particularly, to a method of fabricating a barrier layer on a top surface of metal in damascene structures utilizing ion implantation.

**[0003]** State of the Art: One of the main problems confronting the semiconductor processing industry, in the ultra large scale integration (“ULSI”) age, is that of capacitive-resistance loss in wiring levels. This has led to a large effort to reduce the resistance of, and lower the capacitive loading on, the wiring levels. Since its beginning, the industry has relied on aluminum and aluminum alloys in metallization layers. To improve conductivity in the wiring, it has been proposed that copper metallurgy be substituted for the aluminum metallurgy. However, several problems have been encountered in the development of the copper metallurgy. One of the main problems is the fast diffusion of copper through insulative materials, such as silicon and silicon dioxide (“SiO<sub>2</sub>”), to form an undesired copper oxide compound. In addition, copper is known to cause junction poisoning effects. These problems have led to the development of a liner to separate the copper metallurgy used in the metallization layer from the insulative material. However, copper does not adhere well to oxygen-containing dielectric materials or to itself. Therefore, the liner functions as both an adhesion layer and a barrier layer. In other words, the liner is used to provide adhesion between the copper metallurgy and the insulative material and also to prevent the diffusion of copper through the insulative material.

**[0004]** Liner materials that act as a barrier layer to prevent the diffusion of copper have been investigated by numerous researchers. The use of titanium (“Ti”), zirconium (“Zr”), or hafnium (“Hf”) in the barrier layer has been disclosed. Anonymous, “Improved Metallurgy for Wiring Very

Large Scale Integrated Circuits,” International Technology Disclosures, v. 4 no. 9, (Sep. 25, 1986). Chemical vapor deposition (“CVD”) of titanium nitride (“TiN”) has also been proposed. C. Marcadal *et al.*, “OMCVD Copper Process for Dual Damascene Metallization,” VMIC Conference Proceedings, p. 93-98 (1997). It is currently believed that an optimal liner material for a barrier layer is either a metal, such as tantalum (“Ta”) or tungsten (“W”), or a compound such as tantalum nitride (“Ta<sub>3</sub>N<sub>5</sub>”) or trisilicon tetranitride (“Si<sub>3</sub>N<sub>4</sub>”). Changsup Ryu *et al.*, “Barriers for Copper Interconnections,” Solid State Technology, p. 53-56 (1999).

[0005] Researchers have also proposed an alternate method of forming the barrier layer where the copper of the metallization layer is alloyed with a reactive element, such as aluminum or magnesium. S. P. Muraka *et al.*, “Copper Interconnection Schemes: Elimination of the Need of Diffusion Barrier/Adhesion Promoter by the Use of Corrosion Resistant, Low Resistivity Doped Copper,” SPIE, v. 2335, p. 80-90 (1994) (hereinafter “Muraka”); Tarek Suwwan de Felipe *et al.*, “Electrical Stability and Microstructural Evolution in Thin Films of High Conductivity Copper Alloys,” Proceedings of the 1999 International Interconnect Technology Conference, p. 293-295 (1999). Copper alloys with 0.5 atomic percent aluminum or 2 atomic percent magnesium were used. The reactive element reacted with SiO<sub>2</sub> to form dialuminum trioxide (“Al<sub>2</sub>O<sub>3</sub>”) or magnesium oxide (“MgO”), which acted as a barrier to the further diffusion of the copper into the SiO<sub>2</sub>.

[0006] Similarly, in United States Patent No. 5,130,274 issued to Harper *et al.* (hereinafter “Harper”), an oxide layer that acts as a barrier is disclosed. To form the barrier, a copper alloy containing an alloying element, such as aluminum or chromium, is deposited as a layer. The alloying element reacts with SiO<sub>2</sub> or a polyimide to form an oxide that functions as a barrier compound.

[0007] Semiconductor products that incorporate some of these solutions to the problem of copper diffusion have begun to ship, on a limited basis. However, a problem of how to achieve the lowest possible resistivity in ever smaller lines still remains. As shown in Panos C. Andricacos, “Copper On-Chip Interconnections,” The Electrochemical Society Interface, p. 32-37 (Spring 1999) (hereinafter “Andricacos”), the effective resistivity obtainable by use of barrier layers was approximately 2μΩ-cm with a line width greater than 0.3 μm. The effective resistivity undesirably increases for narrower lines. The alloys investigated by Muraka had similar resistivity values to those found by Andricacos. Muraka also found that the use of 0.5 atomic percent aluminum in the copper was apparently insufficient to provide complete protection from copper diffusion into the

SiO<sub>2</sub>. However, a significant reduction in the rate of copper penetration through the SiO<sub>2</sub> was achieved. The maximum solubility of aluminum in copper is 9.4 weight percent or approximately 18 atomic percent and the maximum solubility of magnesium in copper is 0.61 weight percent or approximately 0.3 atomic percent. Thus, the alloys investigated in Muraka were saturated with magnesium but were far below the saturation limit when aluminum was used as the reactive element.

[0008] Other researchers have investigated the capacitive loading effect with various polymers, such as fluorinated polyimides, to determine if the polymers are possible substitutions for SiO<sub>2</sub> as an insulative material. Several of these polymers have dielectric constants that are considerably lower than the dielectric constant of SiO<sub>2</sub>. However, as in the case with SiO<sub>2</sub>, the polymers also exhibit incompatibility problems with copper metallurgy. It has been shown that polyimide, and many other polymers, react with copper during the curing process to form CuO<sub>2</sub>, which is dispersed within the polymer. D. J. Godbey, L. J. Buckley, A. P. Purdy and A. W. Snow, "Copper Diffusion in Organic Polymer Resists and Inter-level Dielectrics," at the International Conference on Metallurgical Coatings and Thin Films, San Diego, Calif., Apr. 21-25, 1997, Abstract H2.04 p. 313 (hereinafter "Godbey"). CuO<sub>2</sub> is conductive, so its presence raises the effective dielectric constant of the polymer and, in many cases, also increases the conductivity of the polymer.

[0009] Andricacos notes that the use of a copper conductor along with the barrier layer provides a significant improvement in conductivity over the Ti/AlCu/Ti sandwich structure currently used in the industry. Andricacos also noted that as the line width decreases, even a thin barrier layer has a significant effect on the resistance of the composite line. The solutions proposed by Harper and Muraka attempted to address this problem by forming the barrier layer *in situ* by chemically reacting the insulative material and the copper alloy. The barrier layer is formed in the area that was previously the insulative material, leaving the conductor width and height unaffected. However, these processes also affect the resistivity of the conductor because the use of an aluminum alloy, even at a concentration so low as not to be completely effective, shows a measurable increase in resistance compared to that of an unalloyed copper line. While the process of Harper uses only one layer of the copper alloy, the one layer has a significantly high concentration of aluminum and, therefore, the final structure will have an increased resistivity.

[0010] As minimum dimensions shrink, the use of even a 20 Angstrom (“Å”) layer of an alloy having a high resistivity will significantly affect the total resistivity of the conductor composite. For example, a 200Å layer on both sides of a 0.1µm trench is 40 percent of the total trench width. Therefore, at the same time that the dimensions of the conductor element decrease, the specific resistivity increases, which provides a high resistivity at the very time a conductor having a low resistivity is desired.

[0011] It has also been shown that there is a significant difference in the amount of copper oxide formed when a polyimide is used as the insulative material if the acidity of the polymer solution is low. The acidity of the polymer solution is typically low if the precursor used in the formation of the polyimide is an ester instead of an acid. As shown in Godbey, when PI-2701 is used, the amount of oxide formed is reduced by a factor of approximately four in comparison to films that use a similar chemistry but that are prepared from an acid precursor. PI-2701 is a photosensitive polyimide from E.I. du Pont de Nemours & Company (Wilmington, DE) that starts from an ester precursor. It is thought that the slight acidity of PI-2701 comes from the photo-pac or the process used to form it. The films produced in Godbey were prepared by curing the liquid precursor in an air environment or a near, but not completely, inert environment. It is well known that the copper oxide will not form in, and is reduced by, a high purity hydrogen atmosphere.

[0012] Muraka discloses that the use of Ti as a barrier layer was found to increase the resistivity of the copper film significantly when heat-treated at temperatures of 350°C or greater. If the heat treatment was carried out in hydrogen, no increase in resistivity was found. As this temperature is above the eutectoid temperature of a Ti-hydrogen system, the formation of TiH is assumed to have occurred. Muraka also indicates that a similar increase in resistivity is seen with Zr- and Hf-containing copper alloys. However, no data in support of this assertion is provided.

[0013] Other researchers have disputed Muraka’s conclusions. Saarivirta, M.J., “High Conductivity Copper Rich Cu-Zr Alloys,” Transactions of the Metallurgical Society of AIME, 218, p. 431-437, (1960) (hereinafter “Saarivirta”); United States Patent No. 2,842,438 to Saarivirta *et al.* Equilibrium phase diagrams of Cu-Ti and Cu-Zr systems show that the solubility of Zr in copper is more than ten times less than that of Ti. Metals Handbook, v. 8, p. 300-2 (8<sup>th</sup> Ed.). It should also be noted that a series of Cu-Zr alloys have been disclosed that have good electrical conductivity.

[0014] Saarivirta shows that alloys containing more than about 0.01 weight percent of Zr have a significant loss of conductivity in an as-cast state. It has also been shown that the

conductivity of a 0.23 weight percent Zr alloy is restored to above 90 percent of the international annealed copper standard for conductivity ("IACS") when the alloy, in the cold drawn state, is heat-treated above 500° C for one hour. This indicates that a significant amount of the Zr, which was in solid solution in the as-cast state, has precipitated as pentacopper zirconium ("Cu<sub>5</sub>Zr"). Therefore, it can be seen that if the Zr content in the copper is kept low, the conductivity of the resulting metallurgy is above 95 percent of IACS. If a Zr layer is deposited on top of a copper layer, the temperature of deposition of the Zr should be kept below 450° C, with a temperature of 250° C-350° C being preferable. This deposition typically occurs in a single damascene process or at the bottom of vias in a dual-damascene process. When the deposition temperature is kept in this range, a thin layer of Cu<sub>5</sub>Zr tends to form initially, thus inhibiting the diffusion of Zr into the copper. Even at 450° C, the solubility is low enough to provide very good conductivity. Although Zr and Ti have many similar properties, their solubility in copper differs by more than a factor of 10. Therefore, the use of Zr is preferred over Ti for this application.

**[0015]** Methods of forming barrier layers and seed layers by ion implantation are disclosed in United States Patent Nos. 6,420,262 and 6,376,370, both to Farrar, incorporated in their entirety by reference herein. In United States Patent No. 6,420,262, a transition metal, a representative metal, or a metalloid is deposited on an insulator using an ion implantation technique. An inhibiting layer or barrier layer is formed by a reaction between the transition metal, the representative metal, or the metalloid and the insulator. The barrier layer prevents copper from a metallization layer from diffusing into the insulator. In United States Patent No. 6,376,370 a barrier layer and a seed layer are deposited using ion implantation. The barrier layer is formed by depositing Zr, Ti, or Hf by a low energy ion implantation. The seed layer is formed by depositing aluminum, copper, silver, or gold by a low energy ion implantation. Copper, gold, and silver have lower resistivities than aluminum and also have a significantly lower adhesion to oxides than aluminum. However, all of these materials have relatively poor adhesion to polymers.

**[0016]** The processes described above offer significant improvements to the barrier adhesion art for bottom and sidewalls of trenches of a damascene or dual damascene structure. While techniques for forming barrier layers that separate copper from the trenches in a damascene and/or dual damascene structure are known, few acceptable techniques exist for forming the barrier layer on a top surface of a metal in a damascene structure. The few processes that exist require considerable processing and process complexity. For instance, in United States Patent

No. 6,426,289 issued to Farrar, a thin layer of zirconium is deposited on a top surface of a copper metal layer to form a barrier layer. The zirconium is implanted into the copper using a low energy implantation technique. However, the process uses a sacrificial, multilayer dielectric structure and selective etching to form the barrier layer and, therefore, requires modifications to the damascene process.

[0017] It would be desirable to provide a barrier layer for the top surface of a semiconductor device structure that does not require complex processing or modifications to current processes. To reduce processing complexity, it is desirable to form the barrier layer without using a mask to define the barrier layer.

### BRIEF SUMMARY OF THE INVENTION

[0018] The present invention relates to a semiconductor device structure having a barrier layer to prevent the diffusion or penetration of metal. The semiconductor device structure comprises a semiconductor substrate, a dielectric layer, a metallization layer, and the barrier layer. The barrier layer may be a thin layer about 5Å to about 40Å thick formed over the dielectric layer and the metallization layer. The barrier layer may comprise a conductive portion formed from a metal nitride and a nonconductive portion formed from a metal oxide, metal oxynitride, metal carbide, or metal carbonitride. The conductive portion may be present over the metallization layer while the nonconductive portion may be present over the dielectric layer. The metal used in the barrier layer may be Ti, Zr, or Hf. The dielectric layer used in the semiconductor device structure may be an organic material, such as polyimide, or an oxide compound, such as SiO<sub>2</sub>.

[0019] The present invention also relates to a method of forming a barrier layer on a surface of a semiconductor device structure. The method comprises providing a semiconductor substrate and forming a dielectric layer having at least one trench over the semiconductor substrate. A metallization layer is selectively deposited in the trench. A thin metal layer is formed over the metallization layer and the dielectric layer by low energy implantation. The metal layer may be a layer of Ti, Zr, or Hf and be about 5Å to about 40Å thick. The metal layer may be reacted in a nitrogen atmosphere to produce a barrier layer comprising a conductive portion and a nonconductive portion. The conductive portion of the barrier layer may overlie the metallization layer and the nonconductive portion may overlie the dielectric layer. The conductive portion may

comprise a metal nitride and the nonconductive portion may comprise a metal oxide, metal oxynitride, metal carbide, or metal carbonitride.

#### BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

**[0020]** While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

**[0021]** FIG. 1 is a schematic illustration of a cross-sectional view of a semiconductor device structure according to the present invention; and

**[0022]** FIGs. 2A-2E are cross-sectional views of a semiconductor device structure during processing according to the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

**[0023]** The semiconductor device structure of the present invention has a top barrier layer that prevents metal diffusion and contamination. In addition to the top barrier layer, the semiconductor device structure includes a semiconductor substrate, a dielectric or insulative layer, and a metallization layer. The term “top barrier layer” is used herein for convenience to refer to a barrier layer formed over the dielectric layer and the metallization layer. However, it is understood that the barrier layer is not necessarily the top, or uppermost, layer of the semiconductor device structure. Rather, additional layers may be formed over this barrier layer. The top barrier layer may include a conductive layer over the surface of the metallization layer and a nonconductive layer over the dielectric layer. While the top barrier layer prevents metal diffusion, it also provides the semiconductor device structure with a desired, low resistivity since a portion of the top barrier layer is conductive.

**[0024]** The methods and structures described herein do not form a complete process for manufacturing semiconductor device structures. The remainder of the process is known to those of ordinary skill in the art and, therefore, only the process steps and structures necessary to understand the present invention are described herein.

**[0025]** FIG. 1 shows a cross-sectional view of a semiconductor device structure 2 of the present invention. The semiconductor device structure 2 may include a semiconductor substrate 4



having a number of semiconductor devices 6,8. As used herein, the term “semiconductor substrate” includes a semiconductor wafer or other substrate comprising a layer of semiconductor material, such as a silicon wafer, a silicon on insulator (“SOI”) substrate, a silicon on sapphire (“SOS”) substrate, an epitaxial layer of silicon on a base semiconductor foundation, and other semiconductor materials such as silicon-germanium, germanium, gallium arsenide, and indium phosphide.

**[0026]** The semiconductor device structure 2 may optionally include a protective layer 10, which overlies the semiconductor substrate 4. The protective layer 10 prevents metal, such as copper, from contacting the semiconductor devices 6,8. The protective layer 10 may be formed from a silicon nitride compound, such as trisilicon tetranitride (“Si<sub>3</sub>N<sub>4</sub>”). The semiconductor structure 2 may also include contacts 12 that provide electrical connection to the semiconductor devices 6,8. These contacts 12 may include a first barrier layer (or seed layer) 14 and a metal plug 16. The first barrier layer 14 prevents metal from the metal plug 16 from diffusing into the semiconductor devices 6,8.

**[0027]** A dielectric layer 18 may also be present on the semiconductor device structure 2. The dielectric layer may be an inorganic or organic material having a low dielectric constant, such as an oxide compound, an aerogel, or a polymer. The oxide compound may be silicon dioxide (“SiO<sub>2</sub>”). If the dielectric layer 18 is a polymer, the polymer may be an organic polymer that has 5 or more –mer units having carbon chain backbones, an organic oligomer having 2 to 4 –mer units having carbon chain backbones, an organic monomer, or a material having similar properties to those of organic polymers. The polymer may be a polyimide, classes of which are known in the art and described in United States Patent No. 6,077,792 to Farrar. The polymer may include, but is not limited to, a foamed polymer, a fluorinated polymer, and a fluorinated-foamed polymer. Exemplary polymers include, but are not limited to, a DuPont PI-2801 material, a foamed DuPont PI-2801 material, a fluorinated DuPont PI-2801 material, and a fluorinated-foamed DuPont PI-2801 material.

**[0028]** A seed layer 20 and a conductor layer 22, which form a portion of the metallization layer 24, may also be present on the semiconductor device structure 2. A second barrier layer 26 may be present below the seed layer 20 to separate the seed layer 20 and the conductor layer 22 from the dielectric layer 18. As shown in FIG. 1, the dielectric layer 18 may be adjacent to the metallization layer 24.

**[0029]** The top barrier layer 28 may be formed over a top surface of the dielectric layer 18 and the metallization layer 24. While the top barrier layer 28 is illustrated as a single layer, the top barrier layer 28 may, in actuality, include multiple portions. For instance, a portion of the top barrier layer 28 above the metallization layer may be conductive while a portion of the top barrier layer 28 above the dielectric layer 18 may be nonconductive.

**[0030]** The top barrier layer 28 of the semiconductor device structure may be formed on a top surface of the semiconductor device structure 2. FIGS. 2A-2E show cross-sectional views of the semiconductor device structure 2 fabricated according to the present invention. FIG. 2A illustrates a portion of the semiconductor device structure 2 having a number of semiconductor devices 6,8. The semiconductor devices 6,8 may be formed in the semiconductor substrate 4 and include active semiconductor devices 6, such as transistors, and passive semiconductor devices 8, such as capacitors, or a combination of active and passive semiconductor devices 6,8. The semiconductor device structure 2 optionally includes the protective layer 10, which is deposited over the semiconductor substrate 4 and semiconductor devices 6,8. The protective layer 10 may be formed from  $\text{Si}_3\text{N}_4$  and deposited at a thickness of about 100 nm. The dielectric layer 18 may be deposited over the protective layer 10. However, it is also contemplated that the dielectric layer 18 may be formed before the protective layer 10 and, therefore, may be present under the protective layer 10. The thickness of the dielectric layer 18 may depend on the material that is used. For instance, if the dielectric layer 18 is formed from a polymer, the polymer may be deposited to a sufficient thickness to equal a desired thickness of a first wiring level when the polymer is cured. If the dielectric layer 18 is formed from  $\text{SiO}_2$ ,  $\text{SiO}_2$  may be deposited to a thickness that is equal to the desired thickness of the first wiring level.

**[0031]** As shown in FIG. 2B, vias 30 may be opened to semiconductor devices 6,8 using photolithography techniques and etching processes. These photolithography techniques and etching processes are known in the art and may be selected for use in the present invention by a person of ordinary skill in the art. Therefore, the photolithography techniques and etching processes are not presented here in full. The contacts 12, which include the first barrier layer 14 and the metal plug 16, may be formed in the vias 30. The first barrier layer 14 may be deposited in the vias 30 by a suitable deposition technique, such as chemical vapor deposition (“CVD”). The first barrier layer (or seed layer) 14 may be formed from a conventional material, such as titanium silicide. The metal plug 16 may be deposited in the vias 30 by a suitable deposition technique, such as CVD. The

metal plug 16 may be formed from a conventional material, such as W. Excess material from the first barrier layer 14 or the metal plug 16 may be removed from the surface of the dielectric layer 18 or the protective layer 10 by chemical mechanical planarization (“CMP”) or other suitable processes to form a planarized surface.

**[0032]** The dielectric layer 18 may be patterned to define at least one trench 32. As used herein, the term “trench” includes lines for electrically interconnecting semiconductor devices 6,8 in the semiconductor device structure 2. The trench 32 may be formed in the dielectric layer 18 to open up the semiconductor device structure 2 to a number of first level vias, such as vias 30. To form the trench 32, a first level metallization layer pattern may be defined in a photoresist layer formed from a conventional photoresist material. Then, the dielectric layer 18 is etched, using a conventional process, so that the first level metallization layer pattern is defined in the dielectric layer 18. The etching process may include, but is not limited to, reactive ion etching (“RIE”) or an oxide etch. The photoresist layer may subsequently be removed from the semiconductor device structure 2 by a conventional process, such as a wet-strip process, a dry-strip process, or combinations thereof. This process may also remove unwanted portions of the seed layer 20 and the second barrier layer 26, such as portions that are present outside the trench 32 along a top surface of the dielectric layer 18.

**[0033]** As shown in FIG. 2C, the second barrier layer 26 may be deposited on the bottom and sidewalls of the trench 32 and over the top surface of the dielectric layer 18 by conventional techniques, such as low-energy implantation or CVD. The second barrier layer 26 may be formed from tantalum or tantalum nitride. The seed layer 20 may then be deposited over the second barrier layer 26 using CVD, physical vapor deposition (“PVD”), or other methods known in the art. The seed layer 20 may function as a catalyst or a base metal for electroless plating or electroplating of the metallization layer 24. The metal used in the seed layer 20 may be selected depending on the metal to be deposited in metallization layer 24. For instance, if the metallization layer 24 is to be formed from copper, the seed layer 20 may be a copper seed layer. The seed layer 20 may have a thickness of about 100Å.

**[0034]** The remainder of the trench 32 may be filled with a metal using electroless or electrolytic deposition to form the conductor layer 22, which in combination with the seed layer 20 forms the metallization layer 24. As described above, before the metal is deposited, the dielectric layer 18 may be etched to its final shape. For instance, if a dual damascene process is used, both a

line structure and vias may be defined in a single, dielectric layer 18. The metal of the conductor layer 22 may include, but is not limited to, copper, copper alloys, silver, or silver alloys. The conductor layer 22 may be deposited by a selective CVD process, electroplating, or electroless plating. The resulting metallization layer 24 may have a thickness approximately equal to or slightly less than the thickness of the dielectric layer, depending on the material used in the dielectric layer 18. Excess metal may be removed from the metallization layer 24 by CMP.

**[0035]** A thin, metal layer 36 may be deposited on the top surface of the metallization layer 24 and the dielectric layer 18, as shown in FIG. 2D. The metal layer 36 may be deposited at a temperature from about room temperature (approximately 25° C) to about 250° C. The metal may be Ti, Zr, or Hf. To control a thickness of the metal layer 36, the layer may be deposited by a controllable, deposition technique, such as low energy implantation, CVD, or an evaporation technique, which enables the metal to be applied as a thin layer. For instance, the metal layer 36 may be deposited by low energy implantation. An implant energy used during the implantation may be selected so that the metal penetrates the top surface of the metallization layer 24 and the dielectric layer 18. The implant energy may be selected so that a majority of the deposited metal is present in the top few atomic layers of the metallization layer 24 and the dielectric layer 18. The implant energy necessary to penetrate these layers may be from about 0.1 keV to about 2.0 keV, depending on the metal that is to be deposited. To achieve the desired depth, a metal concentration ranging from about  $1.25 \times 10^{16}$  ions/cm<sup>2</sup> to about  $2.0 \times 10^{17}$  ions/cm<sup>2</sup> may be used, depending on the metal to be deposited. The metal may penetrate the metallization layer 24 and the dielectric layer 18 from about 5Å to about 50Å. In other words, the metal layer 36 may be from about 5Å to about 50Å thick. However, it is also understood that the metal may penetrate a different depth into each of the metallization layer 24 and the dielectric layer 18. For instance, the metal may penetrate deeper into the dielectric layer 18 than the metallization layer 24. In one embodiment, the metal layer 36 is from about 5Å to about 40Å thick. However, the thickness of the metal layer 36 may depend on the metal being used. For instance, a zirconium layer from about 10Å to about 30Å thick, or a hafnium layer from about 20Å to about 30Å thick, may be formed.

**[0036]** The metal layer 36 may be reacted to form the top barrier layer 28, which includes a conductive layer 28' and a nonconductive layer 28'', as shown in FIG. 2E. The conductive layer 28' may be formed over the metallization layer 24 and the nonconductive layer 28'' may be formed over the dielectric layer 18. The top barrier layer 28 may be formed by exposing the semiconductor

device structure 2 to a nitrogen-containing environment at a temperature from about 250° C to 450° C. The semiconductor device structure 2 may be exposed to nitrogen for an amount of time sufficient to incorporate nitrogen into portions of the metal layer 36 (FIG. 2D). The nitrogen-containing environment may include, but is not limited to, gases such as nitrogen (“N<sub>2</sub>”), nitric oxide (“NO”), nitrous oxide (“N<sub>2</sub>O”), or ammonia (“NH<sub>3</sub>”). For sake of example only, the semiconductor device structure 2 may be exposed to a nitrogen plasma or an elevated temperature nitrogen treatment, such as a rapid thermal nitrogen treatment. The nitrogen plasma may be generated using a conventional plasma-generating method, such as a method that uses a direct current (“DC”), radiofrequency (“RF”), or microwave power source. The nitrogen plasma may be produced from a gas mixture that includes N<sub>2</sub>, NH<sub>3</sub>, or other nitrogen-containing gases. The semiconductor device structure 2 may be exposed to nitrogen at atmospheric pressure from approximately 0.5 hours to approximately three hours. Longer exposure times may be necessary if only a partial pressure of nitrogen is used.

[0037] To produce the conductive layer 28', portions of the metal layer 36 overlying the metallization layer 24 may react with the nitrogen to produce a conductive, metal nitride compound. For instance, if titanium is used in the metal layer 36, a titanium nitride layer is produced in those portions of the titanium layer overlying the metallization layer 24. At the same time, portions of the metal layer 36 overlying the dielectric layer 18 may react with the carbon or oxygen in the dielectric layer 18 to form the nonconductive layer 28". It is also contemplated that nitrogen may react with the dielectric layer 18 and the portions of the metal layer 36 overlying the dielectric layer 18. Therefore, the nonconductive layer 28" may be formed from a metal oxide, metal oxynitride, metal carbide, or metal carbonitride compound. For instance, if titanium is used as the metal layer 36, a layer of titanium oxide (TiO or TiO<sub>2</sub>) or titanium oxynitride (“TiO(N)<sub>x</sub>”) may be formed over the dielectric layer 18 if that layer includes oxygen. A layer of titanium carbide (“TiC”) or titanium carbonitride (“TiC(N)<sub>x</sub>”) may be formed over the dielectric layer 18 if that layer includes carbon. It is understood that the conductive layer 28' may be zirconium nitride or hafnium nitride and the nonconductive layer 28" may be an oxide, oxynitride, carbide, or carbonitride of zirconium or hafnium if Zr or Hf are deposited as the metal layer 36. The top barrier layer 28 may be about 5 Å to about 100 Å thick.

[0038] Since the nitrogen atmosphere only produces the conductive, metal nitride compound over the metallization layer 24, the conductive layer 28' may be selectively formed over

metal regions of the semiconductor device structure 2 while the nonconductive layer 28" is formed over other regions of the semiconductor device structure 2. Since these portions of the top barrier layer 28 are conductive, a semiconductor device structure 2 having a low resistivity may be produced.

**[0039]** The process described above may be utilized to form a single damascene structure. A dual damascene structure may be constructed using appropriate masking steps known in the art. It is also contemplated that the process may be repeated to form a desired number of metallization layers in the semiconductor device structure 2.

**[0040]** The advantages of the present invention are numerous. First, the top barrier layer 28 prevents metal diffusion and metal penetration in the semiconductor device structure 2. Second, since the top barrier layer 28 is formed by depositing the metal layer 36 and reacting the metal layer 36 in a nitrogen atmosphere, a photomask may not be necessary to define the top barrier layer 28. By eliminating the photomask, the processing complexity of the semiconductor device structure 2 may be substantially reduced. In addition, the formation of the top barrier layer 28 requires no modifications to existing processes, such as a damascene process. Third, the top barrier layer 28 has minimal effect on the total resistivity of the semiconductor device structure 2 because the top barrier layer 28 has a minimal thickness. Fourth, the top barrier layer 28 includes conductive and nonconductive portions, which are selectively formed over the metallization layer 24 and the dielectric layer 18, respectively. Since portions of the top barrier layer 28 are conductive, the semiconductor device structure 2 has the desired, low resistivity.

**[0041]** In one embodiment of the present invention, a semiconductor device structure 2 using copper metallurgy in its entire wiring pattern is formed. A layer of about 100 nm of  $\text{Si}_3\text{N}_4$  is, optionally, deposited over the semiconductor substrate 4 and semiconductor devices 6,8 to form the protective layer 10. The dielectric layer 18, formed from polyimide, is then deposited over the protective layer 10 and cured. The polyimide layer is of sufficient thickness so that its thickness equals the first contact and wiring level of the semiconductor device structure 2 when the polyimide is cured. Contacts 12 are then opened through the polyimide layer and the protective layer. TiN is deposited to form the first barrier layer 14 and W is deposited to form the metal plug 16. Excess W and TiN are subsequently removed from the surface of the protective layer 10 or the polyimide layer by CMP.

**[0042]** A 500Å thick layer of a low temperature oxide or a 500Å thick layer of low temperature  $\text{Si}_3\text{N}_4$  is then deposited, followed by a thin layer of photoresist. The desired damascene images are etched in the oxide or  $\text{Si}_3\text{N}_4$  layer. An oxygen RIE process is used to transfer the desired damascene images into the polyimide layer to define trench 32. The oxygen RIE process also removes portions of the photoresist layer remaining after the damascene images are etched. The seed layer 20 appropriate for the electroless deposition of copper is then deposited. The remaining portions of the oxide or  $\text{Si}_3\text{N}_4$  layer are then removed using an etchant that is selective for these layers but that has negligible effect on the polyimide layer. The etchant also removes the seed layer 20 from any locations outside the trench 32. A layer of copper is selectively electrolessly deposited to form the conductor layer 22. It is also contemplated that the copper layer is deposited by an electroplating process. If electroplating is used, a CMP process is used to remove unwanted copper from the surface of the polyimide layer. The copper layer is deposited in the trench 32 to the same thickness as the trench depth.

**[0043]** The top surfaces of the copper layer and the polyimide layer are implanted with Ti at 0.5 keV and at an implant dose of  $5 \times 10^{16}$  ions/cm<sup>2</sup> to form thin, metal layer 36. The Ti penetrates the copper layer an average of about 10Å and penetrates the polyimide layer about 30Å. The Ti layer is then exposed to a nitrogen plasma at 350°C for one hour. Portions of the Ti layer overlying the copper layer react with the nitrogen to form a TiN layer while portions of the Ti layer overlying the polyimide layer form a TiC or  $\text{TiC}(\text{N})_x$  layer. This process is repeated as necessary to build a multi-level, copper polyimide wiring structure having a desired number of layers. Depending on a temperature used to apply and cure the polyimide, as well as a temperature used to deposit the photoresist layer, a final post-processing heat treatment of 250°C-350°C for approximately 1 to 2 hours may be used to achieve the lowest resistivity conductors.

**[0044]** In another embodiment, the dielectric layer 18 is formed from  $\text{SiO}_2$ . A layer of approximately 100 nm of  $\text{Si}_3\text{N}_4$  is, optionally, deposited over the semiconductor substrate 4 and semiconductor devices 6,8 to form the protective layer 10. In this embodiment, the dielectric layer 18, formed from  $\text{SiO}_2$ , is formed over the  $\text{Si}_3\text{N}_4$  layer. Contacts 12 are then opened through the  $\text{SiO}_2$  layer and the protective layer. TiN is deposited to form the first barrier layer 14 and W is deposited to form the metal plug 16. Excess W and TiN are subsequently removed from the surface of the protective layer 10 or the  $\text{SiO}_2$  layer by CMP. An additional oxide layer is then applied having a thickness equal to the desired thickness of the first wiring level.

**[0045]** A 500Å thick layer of low temperature Si<sub>3</sub>N<sub>4</sub> is then deposited, followed by a thin layer of photoresist. The desired damascene images are etched in the Si<sub>3</sub>N<sub>4</sub> layer and an oxide etch is used to transfer the desired damascene images into the SiO<sub>2</sub> layer to define trench 32. The seed layer 20 appropriate for the electroless deposition of copper is then deposited. The photoresist layer is then removed using a selective etchant having negligible effect on the SiO<sub>2</sub> layer. A copper layer is selectively electrolessly deposited to form the conductor layer 22. The thickness of the copper layer is slightly less than the thickness of the SiO<sub>2</sub> layer. In other words, the nominal copper thickness plus the deposition tolerance equals the thickness of the SiO<sub>2</sub> layer. The surface of the copper layer is then implanted with Ti at 0.5 keV. The Ti penetrates the copper layer an average of about 10Å and penetrates the oxide layer about 20Å. An implant dose of 5x10<sup>16</sup> ions per square cm is used. The Ti layer may be deposited by any other means desired. The Ti layer is exposed to a nitrogen plasma at 350°C to form a TiN layer on the copper layer and a TiO, TiO<sub>2</sub>, or TiO(N)<sub>x</sub> layer on the SiO<sub>2</sub> layer.

**[0046]** While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope thereof as defined by the following appended claims.